1. An integrated circuit that processes a communication packet, the integrated circuit comprising:

a core processor configured to execute a software application that directs the core processor to process the communication packet; and

scheduling circuitry configured to retrieve first scheduling parameters cached in a context buffer for the packet and execute a first algorithm based on the first scheduling parameters to schedule subsequent transmission of the communication packet.

2. The integrated circuit of claim 1 wherein the scheduling circuitry is configured to retrieve second scheduling parameters cached in the context buffer, and concurrently with the execution of the first algorithm, execute a second algorithm based on the second scheduling parameters to schedule the subsequent transmission of the communication packet.

3. The integrated circuit of claim 2 wherein the first algorithm and the second algorithm comprise guaranteed cell rate algorithms.

4. The integrated circuit of claim 1 wherein scheduling circuitry is configured to update the first scheduling parameters and write the updated scheduling parameters to the context buffer.

5. The integrated circuit of claim 1 wherein the first scheduling parameters indicate a first one of the priority levels and a second one of the priority levels, wherein the first

priority level has a higher priority than the second priority level, and wherein the scheduling circuitry is configured to first attempt to schedule the transmission of the communication packet with the second priority level, and if unsuccessful, then to attempt to schedule the transmission of the communication packet with the first priority level.

6. The integrated circuit of claim 1 wherein the first scheduling parameters are automatically cached by co-processor circuitry in the context buffer.

7. The integrated circuit of claim 1 wherein a highest one of the priority levels is for scheduling constant bit rate traffic.

8. The integrated circuit of claim 7 wherein a lowest one of the priority levels is for scheduling available bit rate traffic.

9. The integrated circuit of claim 1 wherein a first one of the priority levels is for scheduling real-time traffic, a second one of the priority levels is for scheduling non-real-time traffic, and wherein the first priority level has a higher priority than the second priority level .

10. The integrated circuit of claim 1 wherein the scheduling circuitry is configured to operate in parallel with the core processor.

11. A method of operating an integrated circuit to process a communication packet, the method comprising:

in a core processor, executing a software application that directs the core processor to process the communication packet; and

in scheduling circuitry, retrieving first scheduling parameters cached in a context buffer for the packet and executing a first algorithm based on the first scheduling parameters to schedule subsequent transmission of the communication packet.

12. The method of claim 11 further comprising, in the scheduling circuitry, retrieving second scheduling parameters cached in the context buffer, and concurrently with the execution of the first algorithm, executing a second algorithm based on the second scheduling parameters to schedule the subsequent transmission of the communication packet.

13. The method of claim 12 wherein the first algorithm and the second algorithm comprise guaranteed cell rate algorithms.

14. The method of claim 11 further comprising, in the scheduling circuitry, updating the first scheduling parameters and writing the updated scheduling parameters to the context buffer.

15. The method of claim 11 wherein the first scheduling parameters indicate a first one of the priority levels and a second one of the priority levels, wherein the first priority level

has a higher priority than the second priority level, and wherein executing the first algorithm based on the first scheduling parameters to schedule the subsequent transmission of the communication packet comprises first attempting to schedule the transmission of the communication packet with the second priority level, and if unsuccessful, then attempting to schedule the transmission of the communication packet with the first priority level.

16. The method of claim 11 wherein the first scheduling parameters are automatically cached by co-processor circuitry in the context buffer.

17. The method of claim 11 wherein a highest one of the priority levels is for scheduling constant bit rate traffic.

18. The method of claim 17 wherein a lowest one of the priority levels is for scheduling available bit rate traffic.

19. The method of claim 11 wherein a first one of the priority levels is for scheduling real-time traffic, a second one of the priority levels is for scheduling non-real-time traffic, and wherein the first priority level has a higher priority than the second priority level .

20. The method of claim 11 wherein the scheduling circuitry operates in parallel with the core processor.